Notice of Allowability	Application No. 10/808,079	Applicant(s) MORIOKA, MAKOTO	
	Examiner Thang V. Tran	Art Unit 2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *a communication dated 03/24/04*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: claims 1-20 are allowed over the prior art of record because the all of references of the prior art, considered alone or in combination, fails to suggest or fairly teach a write strategy circuit for capturing input data to be written on an optical disk including a combination of: a strategy clock generator configured to generate a strategy clock signal by multiplying a frequency of a channel clock signal; a phase controller configured to produce a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal; a data capturing circuit configured to capture the input data in synchronization with the capturing channel clock signal; a phase determination circuit configured to determine whether a length of the input data corresponds to a predetermined value; and a strategy correction circuit configured to apply a predetermined strategy correction to the input data based on the strategy clock signal, wherein the phase controller controls the phase of the channel clock signal according to a determination result of the phase determination circuit, as recited in claim 1; or a write strategy method for capturing input data to be written on an optical disk including a combination of steps: first generating a strategy clock signal by multiplying a frequency of a channel clock signal; first producing a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal; capturing the input data in synchronization with the capturing channel clock signal; determining whether a length of the input data corresponds to a predetermined value; and applying a predetermined strategy correction to the input data based on the strategy clock signal, wherein the first producing step controls the phase of the channel clock signal according to a determination result of the determining step, as recited in claim 6; or

a write strategy circuit for capturing input data to be written on an optical disk includes a combination of: first generating means for generating a strategy clock signal by multiplying a frequency of a channel clock signal; first producing means for producing a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal; means for capturing the input data in synchronization with the capturing channel clock signal; determining means for determining whether a length of the input data corresponds to a predetermined value; and means for applying a predetermine strategy correction to the input data based on the strategy clock signal, wherein the first producing means controls the phase of the channel clock signal according to a determination result of the determining means, as recited in claim 11; or an optical disk apparatus for capturing input data to be written on an optical disk including a combination of: a write strategy circuit including: a strategy clock generator configured to generate a strategy clock signal by multiplying a frequency of a channel clock signal; a phase controller configured to produce a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal; a data capturing circuit configured to capture the input data in synchronization with the capturing channel clock signal; a phase determination circuit configured to determine whether a length of the input data corresponds to a predetermined value; and a strategy correction circuit configured to apply a predetermined strategy correction to the input data based on the strategy clock signal, wherein the phase controller controls the phase of the channel clock signal according to a determination result of the phase determination circuit, as recited in claim 16. Claims 2-5, 7-10, 12-15, 17-20 are allowed with their respective parent claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CITED REFERENCES

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate to an optical apparatus having a write strategy circuit for processing data to be recorded on an optical recording medium.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang V. Tran whose telephone number is (571) 272-7595. The examiner can normally be reached on M-F 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Hoa can be reached on (571) 272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thang V. Tran
Primary Examiner
Art Unit 2627